

Pyxis NexusRoute-SoC

Next Generation Router for Advanced Technology Design

Architected to Address sub-45nm Design Rules

Simultaneously Optimizes Runtime, DRCs, Timing, SI, Power and Yield

Industry Integrated One-pass Gridded Routing with Concurrent Shape-based DRC Fixing

Multi-million Gate Capacity with Multi-threaded and Distributed Performance

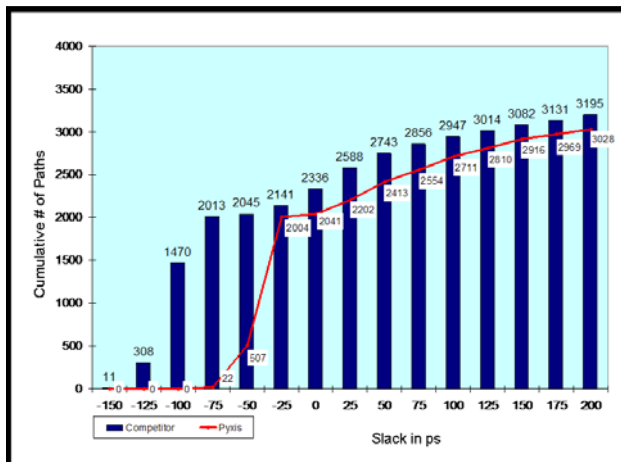
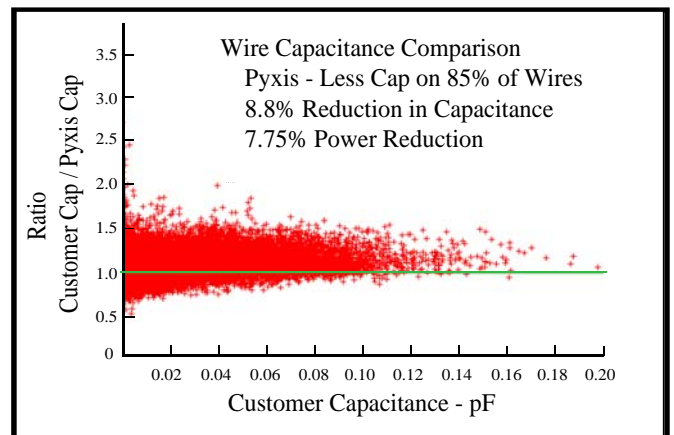
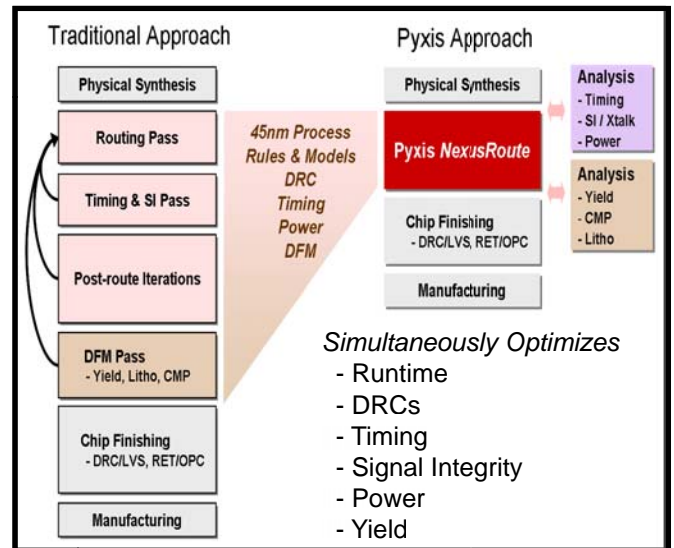
Advanced Technology Design Closure New Game, New Rules, New Technology

At advanced technology nodes design closure is a new game with new rules. An exponential increase in the number of design rules to be comprehended makes design closure very difficult. These new rules are causing longer router runtimes and forcing designers to do more iterations to clean up remaining DRC violations. Unlike existing routers, which use multiple rip-up and re-route sequences that leave 1000's of DRCs, *NexusRoute-SoC* uses a new architecture that does concurrent DRC fixing during routing to provide orders of magnitude cleaner designs in a single pass.

Faster Closure For Sub-45nm Designs

NexusRoute-SoC is specifically architected to speed design closure at 45nm and below. It uses a single-pass approach that concurrently optimizes runtime, DRCs, timing, signal integrity, power and yield. With this approach all design metrics are optimized concurrently with the routing, thus reducing turnaround time and the number of iterations required to close the design.

NexusRoute-SoC also uses best-in-class global routing technology, providing a powerful planning function that takes into account the design of the metal stack, congestion and blockages and allocates the route spacing necessary to meet performance and power goals. This planning is adhered to by the detailed router to ensure a one-pass routing flow with no surprises. With Pyxis, what you plan is what you get.



Better IC Performance & Power

NexusRoute-SoC uses multi-corner, multi-mode analysis to proactively identify timing and SI-critical signals and then concurrently performs a powerful set of optimizations to avoid timing issues during routing. *NexusRoute-SoC* also employs 3D wire balancing and the ability to optimize the routing of frequently switching signals to enhance design performance, improve timing margins and reduce power consumption.

NexusRoute-SoC provides the user with complete control of all routing constraints for the most performance demanding designs.



Pyxis NexusRoute-SoC

Next Generation Architecture for 45nm Design Closure

3D Wire Balancing & 2D Wire Spreading for Superior Performance, Power and Yield
 Correct-by-construction with Concurrent Shape-based DRC Fixing for Cleaner Designs
 Cost-based Incremental Routing for Fast ECOs
 Multi-threaded / Distributed Processing for Scalability to Large SoC Designs

3D Wire Balancing & 2D Wire Spreading

Conventional routers build the routing from the bottom layers up and do wire spreading as a post-route optimization. *NexusRoute-SoC* is architected to achieve superior results through a more efficient use of the entire routing space. 2D spreading is planned at the global route stage and *NexusRoute-SoC* balances the wires across all of the available layers (see figure) to free up space in the lower metal levels. This results in less congestion, shorter wire length, fewer vias and better spreading of wires, all of which improves performance of the chip by reducing wire parasitics. We call this 3D wire balancing and it's unique in the industry.

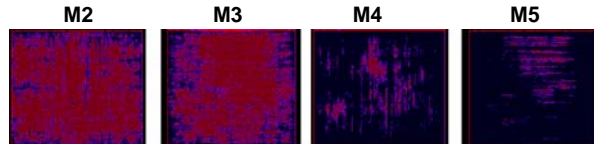
Cost-based Incremental Routing

NexusRoute-SoC has patent-pending algorithms that can opportunistically make trade-offs between hard and soft design rules, giving the user unprecedented control of how the router handles critical signals. The router also incrementally makes ECO changes fast and predictable, with minimal changes to the rest of the design.

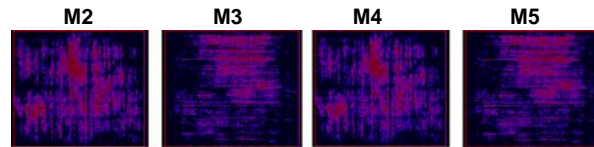
Design Flow Integration and Correlation

NexusRoute-SoC is architected to add value to the flows of leading EDA companies such as Cadence, Magma and Synopsys. *NexusRoute-SoC* natively uses OpenAccess and standard file formats to provide seamless transfer of placement, routing and constraint data for full routing.

NexusRoute-SoC includes integrated extraction, timing and DRC engines that are correlated to industry standard sign-off tools such as STAR-RC, PrimeTime-SI, Hercules and Calibre.



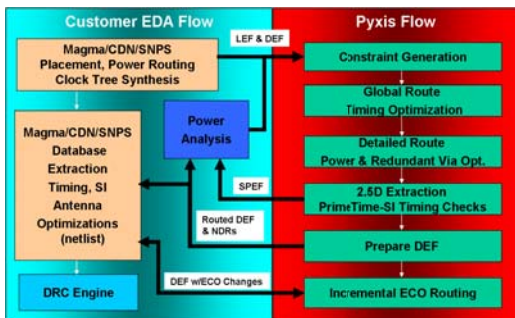
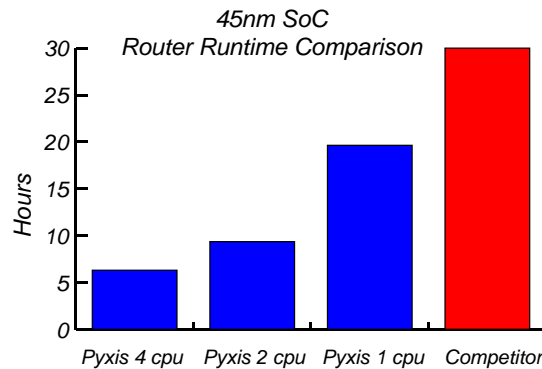
Congestion maps for traditional router.



Congestion maps for Pyxis with 3D Balancing.

Multi-threaded / Distributed Processing

The *NexusRoute-SoC* architecture provides the scalability and capacity to route multi-million net designs using both multi-threaded and distributed processing. Unlike conventional routers whose quality of results and DRC violations suffer with design partitioning, *NexusRoute-SoC* delivers clean designs with superior quality of results even when partitioning the design for multi-processing.



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SPECIFICATIONS

Inputs

- User Constraints through Tcl
- Liberty™: Timing/Logical Library
- SDC™: Timing Constraints
- Verilog™: Logical Connectivity
- LEF™: Cell Abstracts, Rules
- DEF™: Floorplan, Connectivity and Detailed Placement
- DFM Properties: Advanced soft and hard design rules
- Process Layer Thickness and Dielectrics
- OpenAccess™

Outputs

- Verilog™: Logical Netlist
- LEF™: Cell Abstracts, Rules
- DEF™: Floorplan, Netlist, Placement and Routing
- SPEF™: RC Parasitics
- GDSII™: Routed Polygons
- OpenAccess™

Platforms

- Linux 32-bit: RHEL3, Fedora2,
- Linux 64-bit (X86_64): RHEL3, Fedora2,