

Pyxis NexusRoute-HPC

Next Generation Router for High Performance Custom Design

- Automated Custom Routing Slashes Cycle Time From Weeks to Minutes
- Hierarchical Routing Integrated into Full Custom Chip Editing Environments
- One Pass Routing with Concurrent Shape-based DRC Fixing
- Integrated Parasitic Extraction for Rapid What-If Analysis

Automated Routing for Custom Design Slashes Cycle Time From Weeks to Minutes

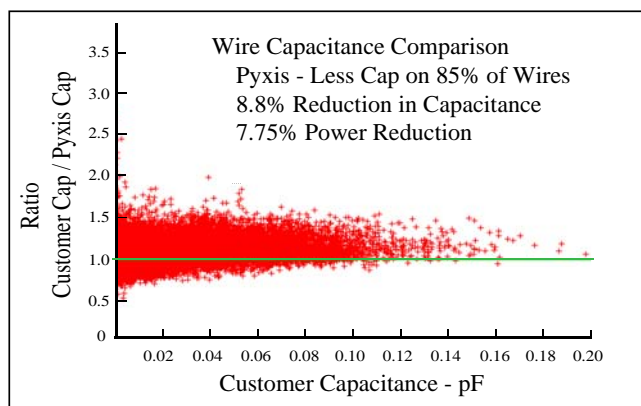
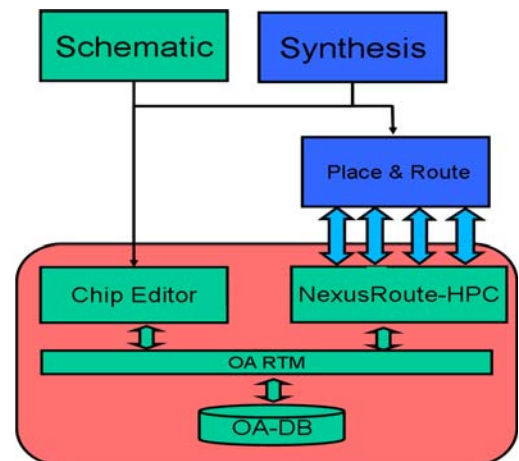
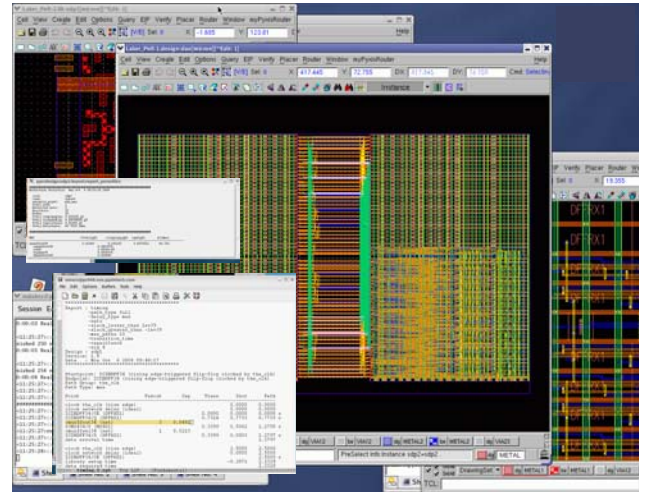
Custom designers pushing the edge of technology are finding it difficult to move their designs to advanced technology nodes due to the exponential increase in the number and complexity of design rules that must be comprehended. Manual layout of signal lines for custom blocks can take weeks and the new design rules are forcing the designer to do more iterations to clean up remaining DRC violations.

Unlike manual layout, *NexusRoute-HPC* provides the designer with automated correct-by-construction routing that can route custom blocks in minutes. *NexusRoute-HPC* uses concurrent shape-based DRC fixing while routing to provide orders of magnitude cleaner designs in a single layout pass.

Hierarchical Routing in a Chip Editor

NexusRoute-HPC is architected for hierarchical custom design environments. Unlike other routers that work on flat data and require abstracts for instances of lower level cells in the hierarchy, *NexusRoute-HPC* can accommodate large fully-hierarchical designs and route them DRC clean in the context of geometries from lower levels of the design hierarchy.

NexusRoute-HPC runs natively on the industry standard OpenAccess (OA) database and can be loaded into any chip editor that uses the OA runtime model (RTM). The router can do area-based operations and has built in analysis engines giving the designer the ability to rapidly manipulate his design and try several different layout scenarios to achieve an optimum design.



Better IC Performance & Power

NexusRoute-HPC provides the user with complete control of all routing constraints for the most performance demanding designs. *NexusRoute-HPC* uses 3D wire balancing and the ability to optimize the routing of frequently switching signals to enhance design performance, improve timing margins and reduce power consumption.



Pyxis NexusRoute-HPC

Next Generation Architecture for Custom Design Routing

3D Wire Balancing & 2D Wire Spreading for Superior Performance, Power and Yield
Correct-by-construction with Concurrent Shape-based DRC Fixing for Cleaner Designs
Integrated Extraction & Timing Engines with Incremental Routing for Fast What-If Analysis
Compatible with OA-based Pycell Interoperable PDK Libraries

3D Wire Balancing & 2D Wire Spreading

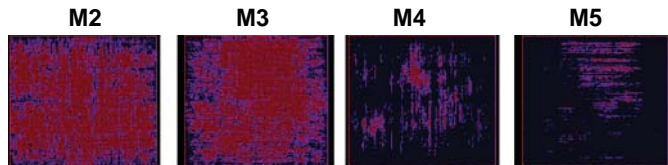
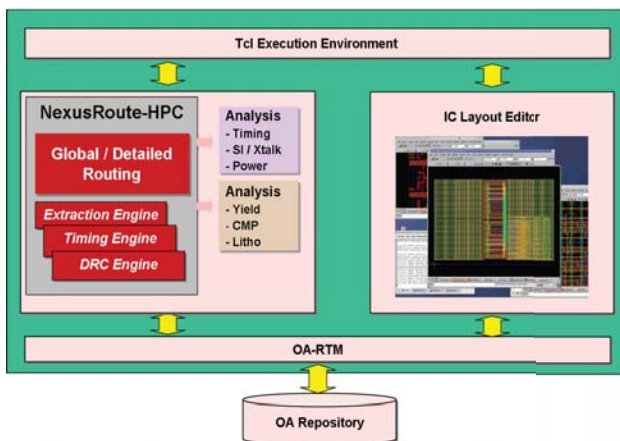
Unlike conventional routers that build routing from the bottom layers up and do wire spreading as a post-route optimization, *NexusRoute-HPC* achieves superior routing results by balancing the wire length used at all levels of the hierarchy across all of the available layers (see figure) to free up space in the lower metal layers. This results in improved IC performance by reducing wire parasitics. We call this 3D wire balancing and it's unique in the industry.

Incremental Routing with Integrated Analysis

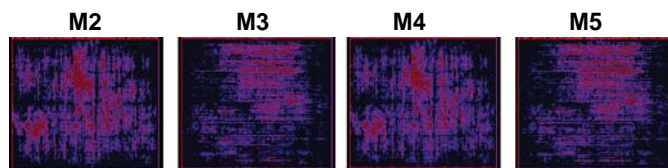
NexusRoute-HPC is an incremental router with patent-pending algorithms that can opportunistically make trade-offs between hard and soft design rules, giving the user unprecedented control of how the router handles critical signals. The router also has integrated extraction and timing engines enabling the user to do fast "what-if" scenarios to find optimal routing topologies. The incrementally of the router makes changes fast and predictable, with minimal impact to the rest of the design.

Integration With Chip Editors Ideal for Chip Finishing & ECOs

NexusRoute-HPC is architected to add value to the custom chip editing environments of leading EDA companies such as Cadence, Magma, Springsoft and Synopsys. *NexusRoute-HPC* natively uses OpenAccess to seamlessly integrate directly into these custom chip editing environment making it an excellent routing tool for timing-aware chip finishing and ECOs.



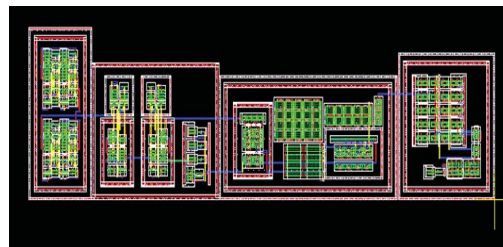
Congestion maps for traditional router.



Congestion maps for Pyxis with 3D Balancing.

All *NexusRoute-HPC* functionality including routing, parasitic extraction, timing analysis, signal and DFM optimization are available from within the chip editing environment. Once integrated, all design edits made in the layout editor are immediately seen by the router and visa-versa with no need for data translation.

NexusRoute-HPC is also compatible with OA-based Pycells from Ciranova that are used to build Interoperable PDK Libraries.



Example of Ciranova Pycell Based PLL Circuit Routed with NexusRoute-HPC

SPECIFICATIONS

Inputs

- User Constraints through Tcl
- Liberty™: Timing/Logical Library
- SDC™: Timing Constraints
- Verilog™ : Logical Connectivity
- LEF™: Cell Abstracts, Rules
- DEF™: Floorplan, Connectivity and Detailed Placement
- DFM Properties: Advanced soft and hard design rules
- Process Layer Thickness and Dielectrics
- OpenAccess™

Outputs

- Verilog™: Logical Netlist
- LEF™: Cell Abstracts, Rules
- DEF™: Floorplan, Netlist, Placement and Routing
- SPEF™: RC Parasitics
- GDSII™: Routed Polygons
- OpenAccess™

Platforms

- Linux 32-bit: RHEL3, Fedora2,
- Linux 64-bit (X86_64): RHEL3, Fedora2,

For more information, please contact us at sales@pyxistech.com or call us at (512) 637-0500.

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